

Fig.1

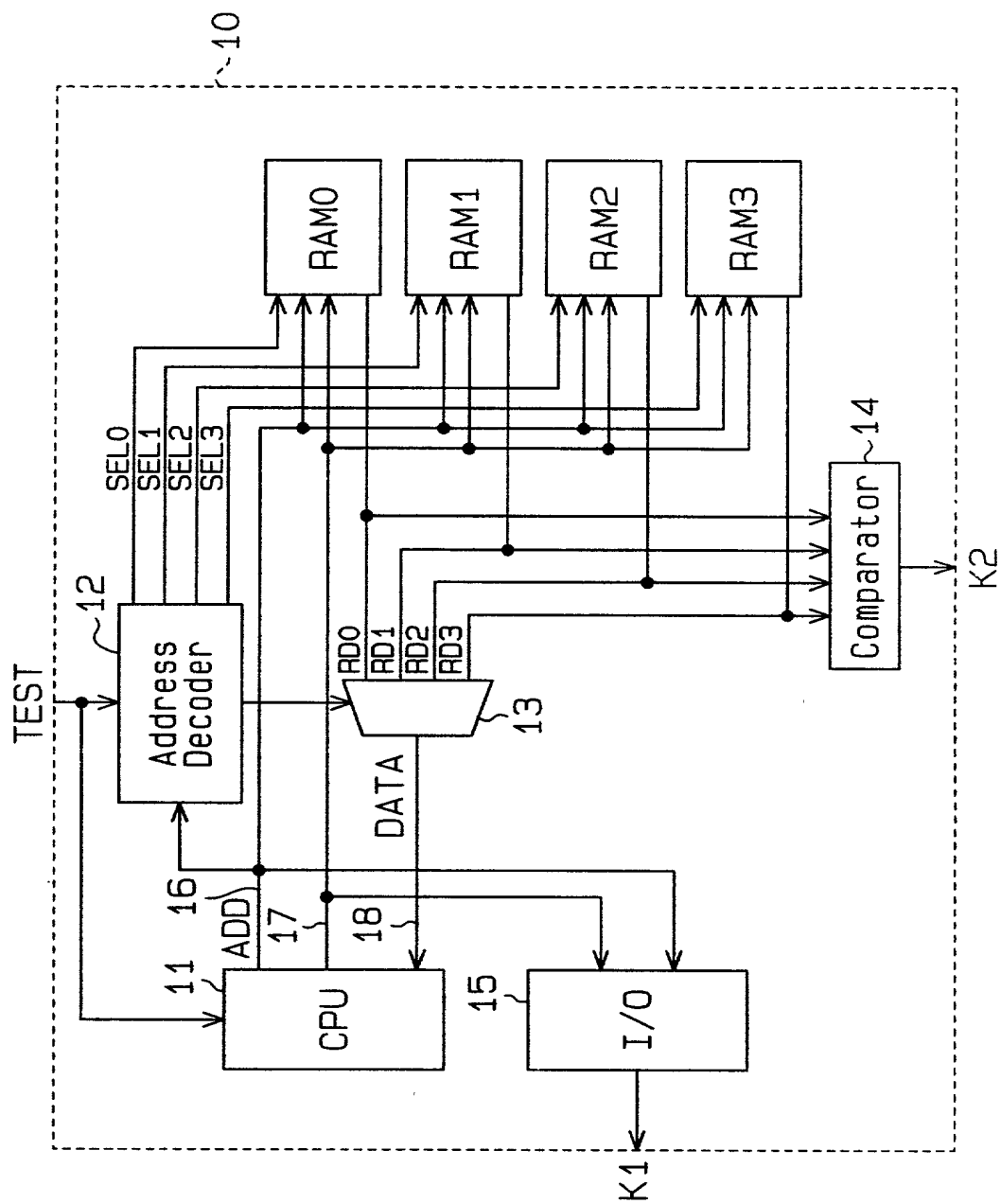


Fig.2

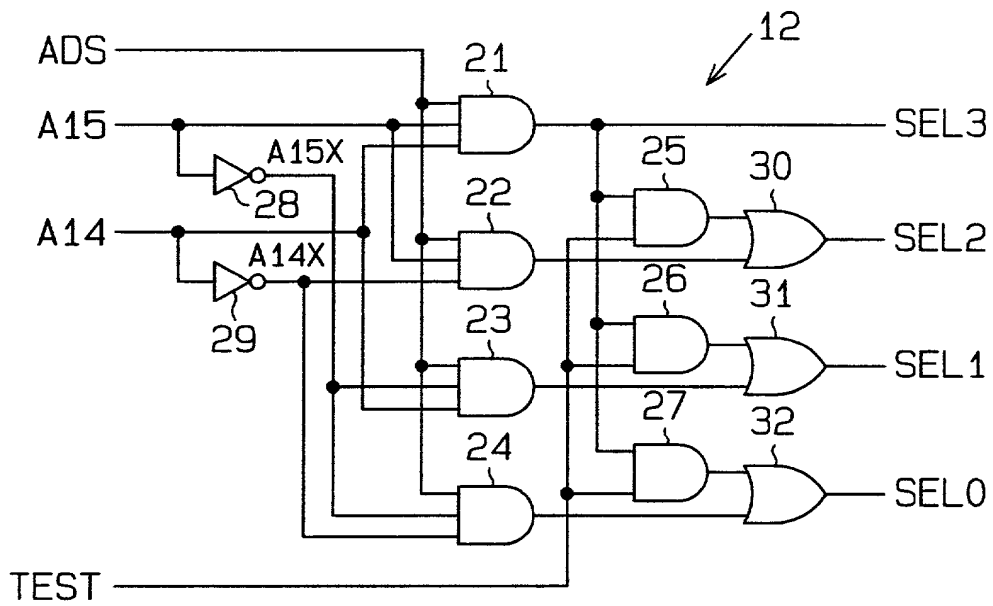


Fig.3

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	0
1	0	0	1	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1
0	X	X	X	0	0	0	0

Fig. 4

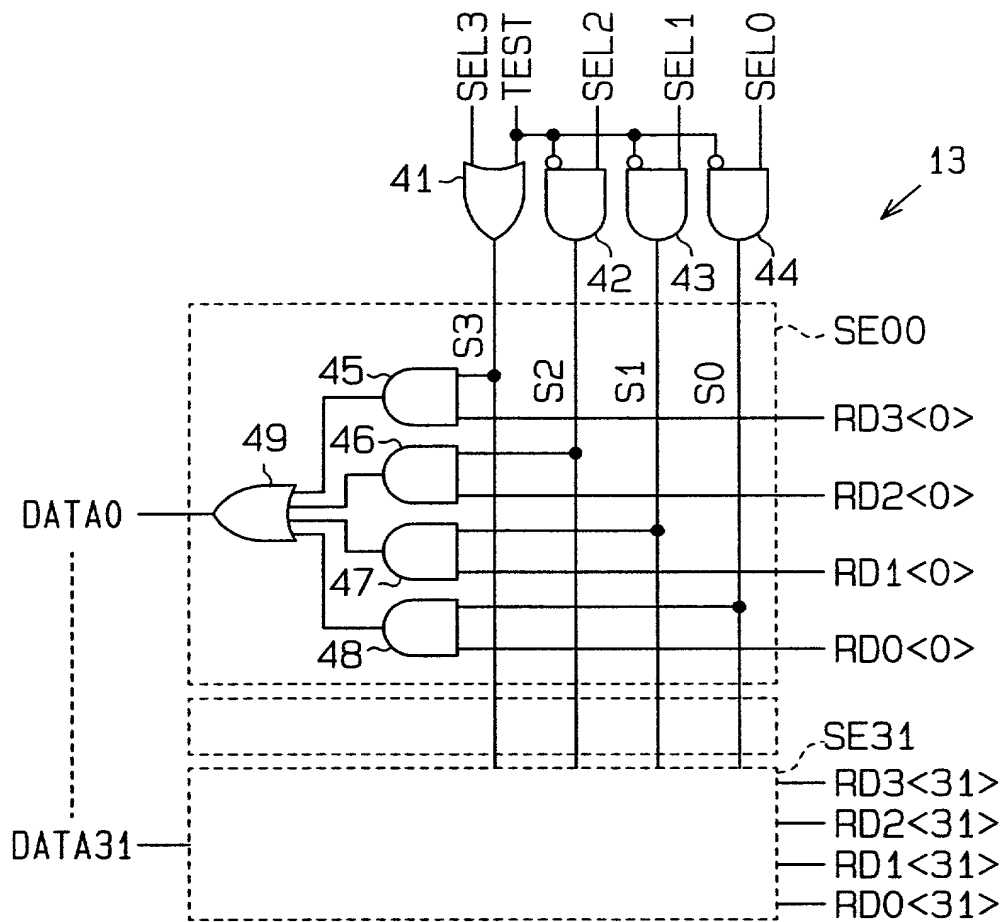


Fig. 5

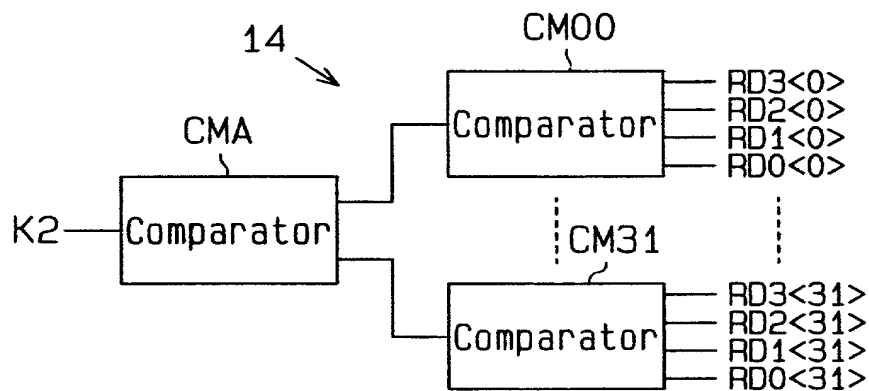


Fig.6

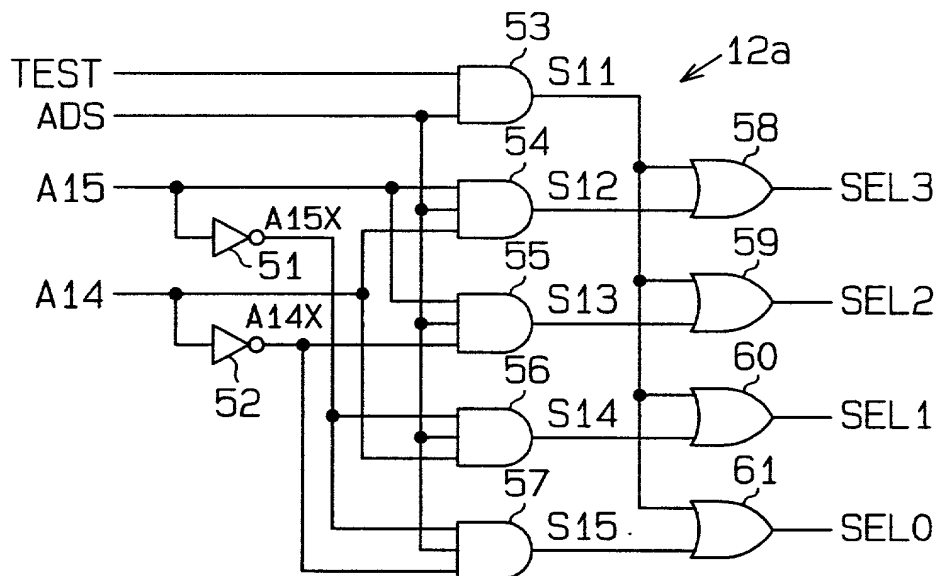


Fig.7

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	0
1	X	X	1	1	1	1	1
0	X	X	X	0	0	0	0

Fig. 8

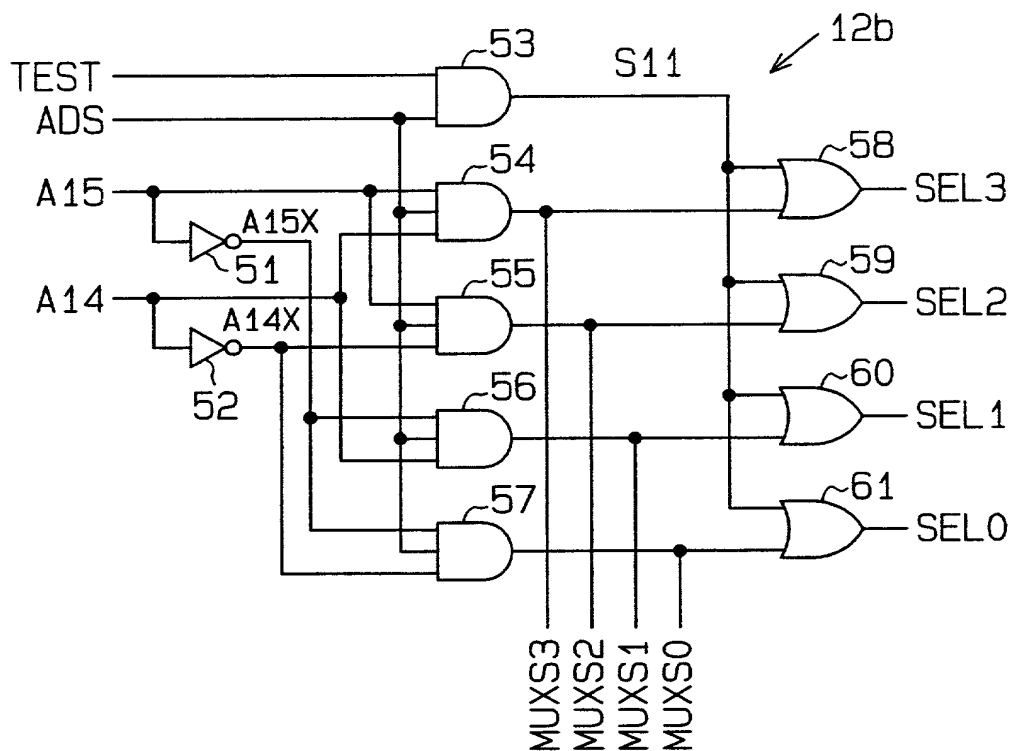


Fig. 9

Upper Address Decode Signal	A15	A14	TEST	SEL3	SEL2	SEL1	SELO
1	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0
1	1	0	0	0	1	0	0
1	1	1	0	1	0	0	0
1	X	X	1	1	1	1	1
0	X	X	X	0	0	0	0

Fig.10

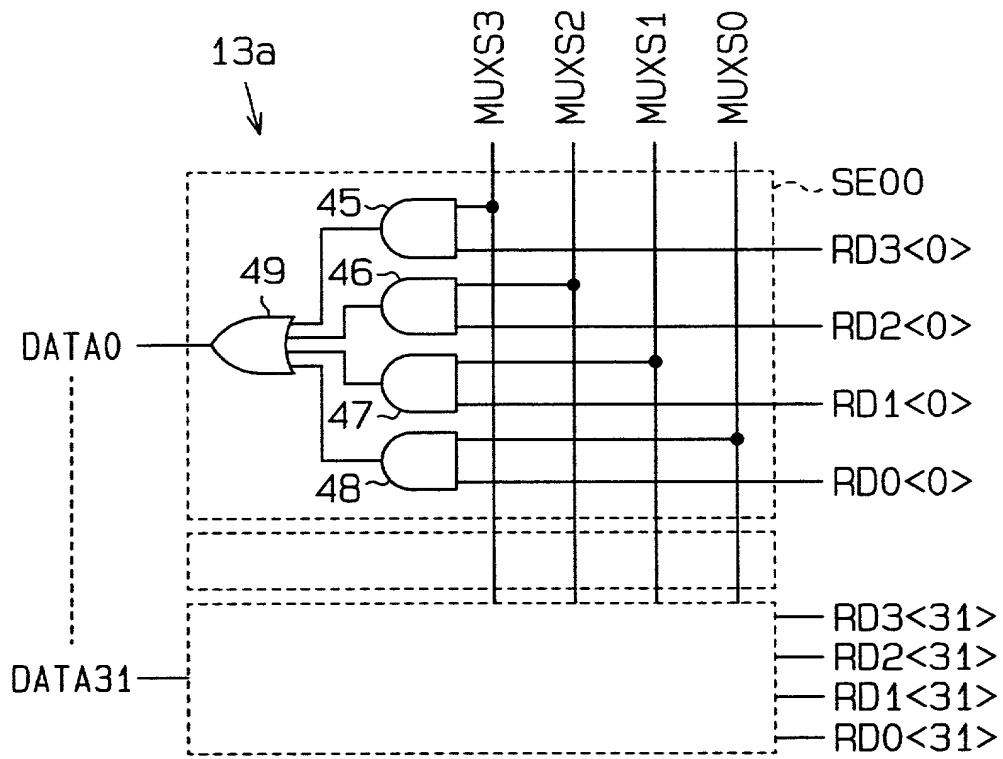


Fig.11

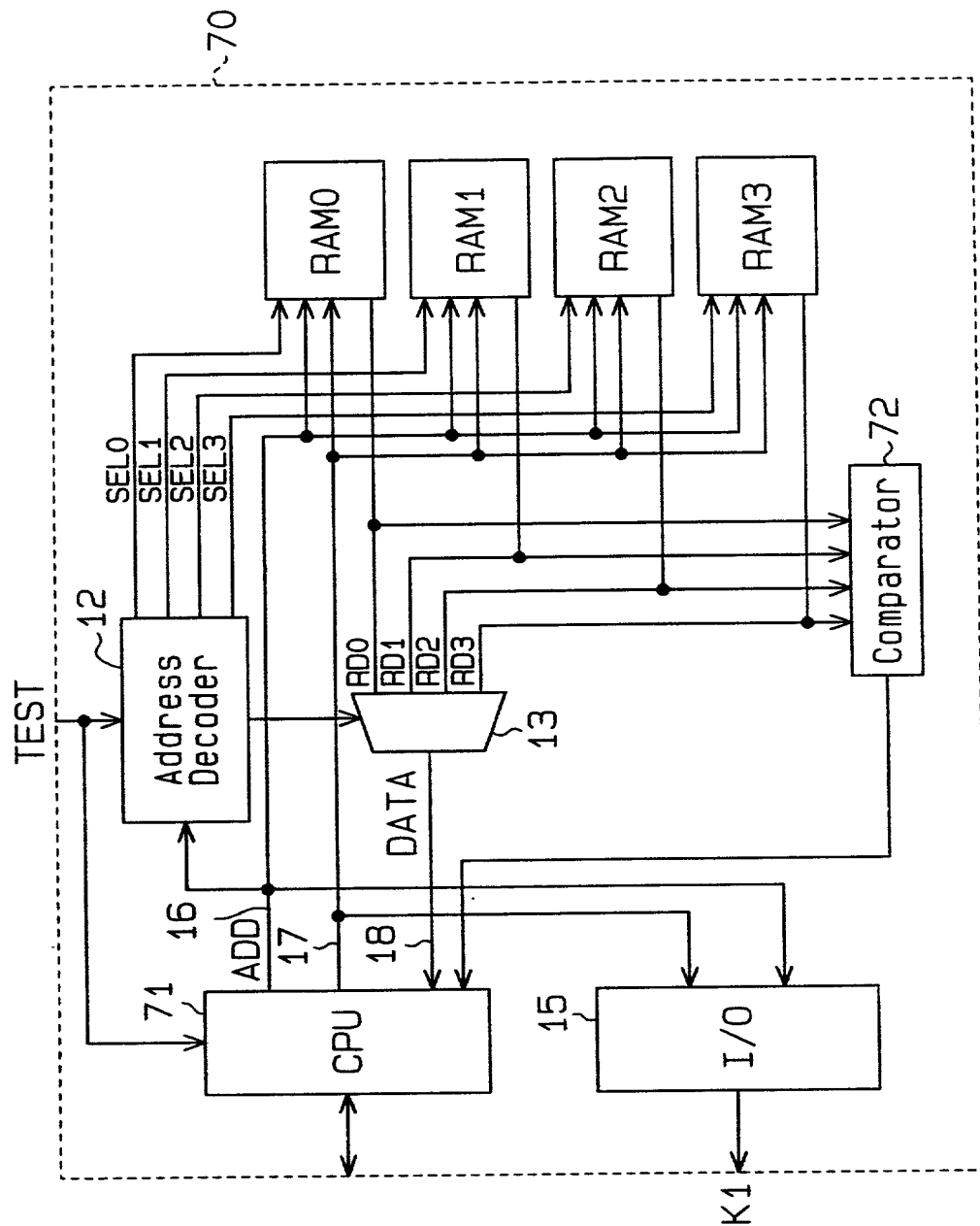


Fig.12

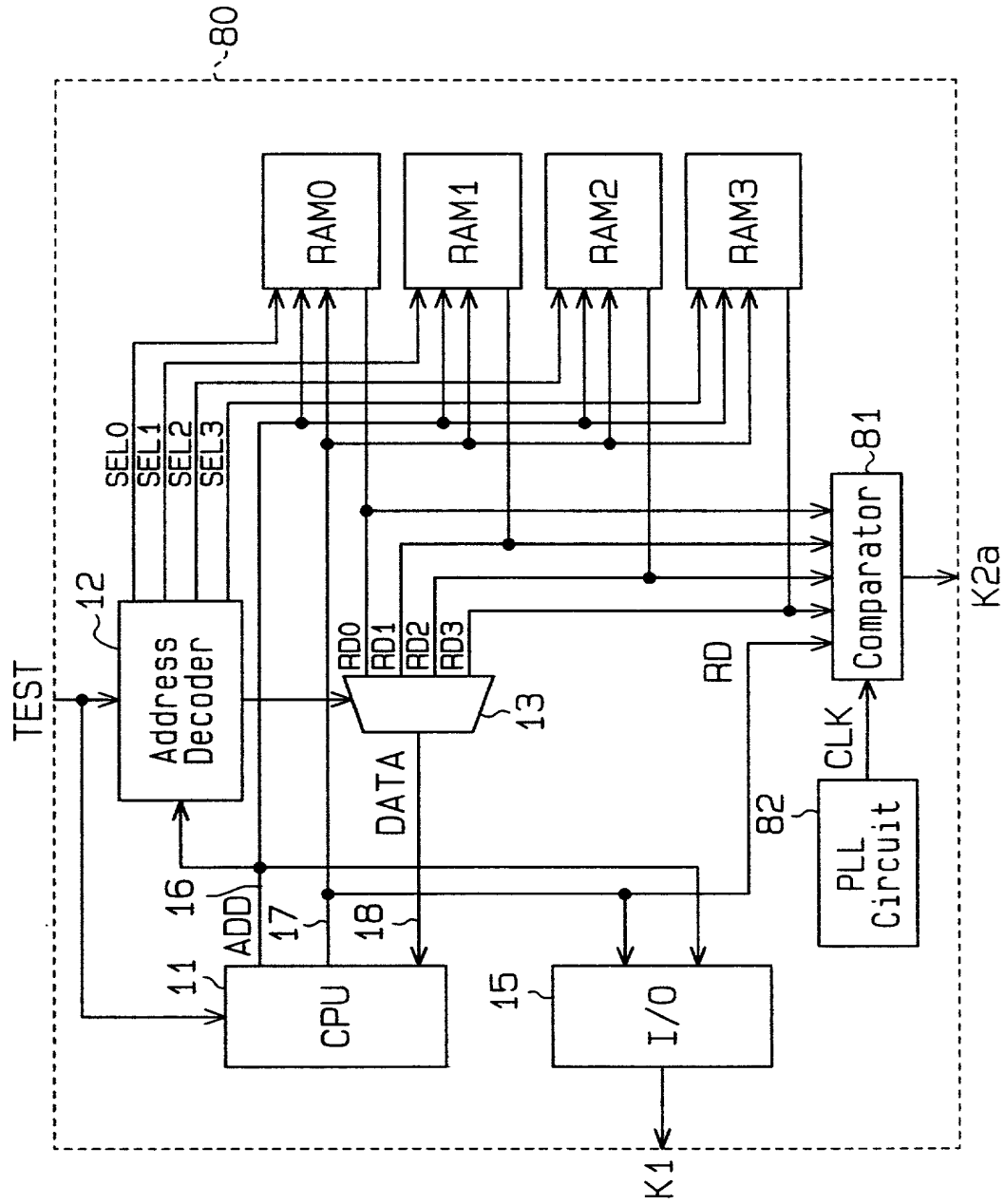


Fig.13

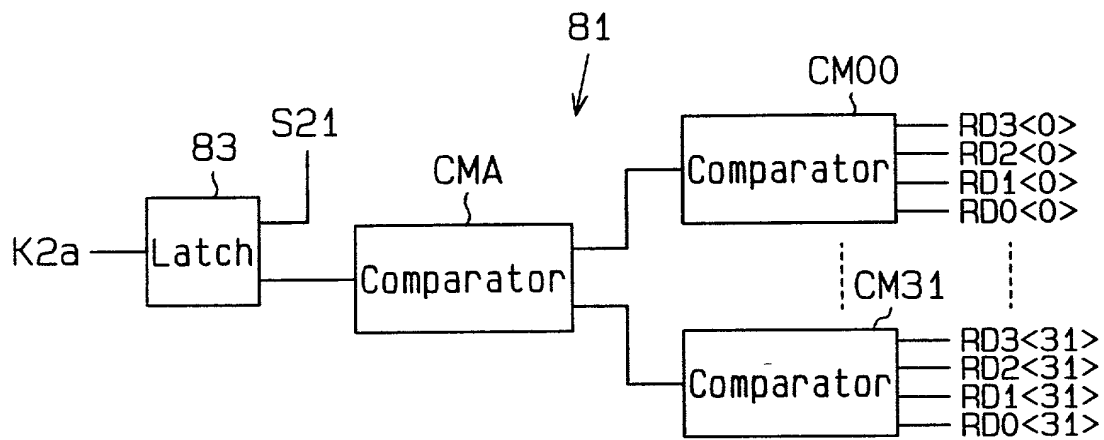


Fig.14

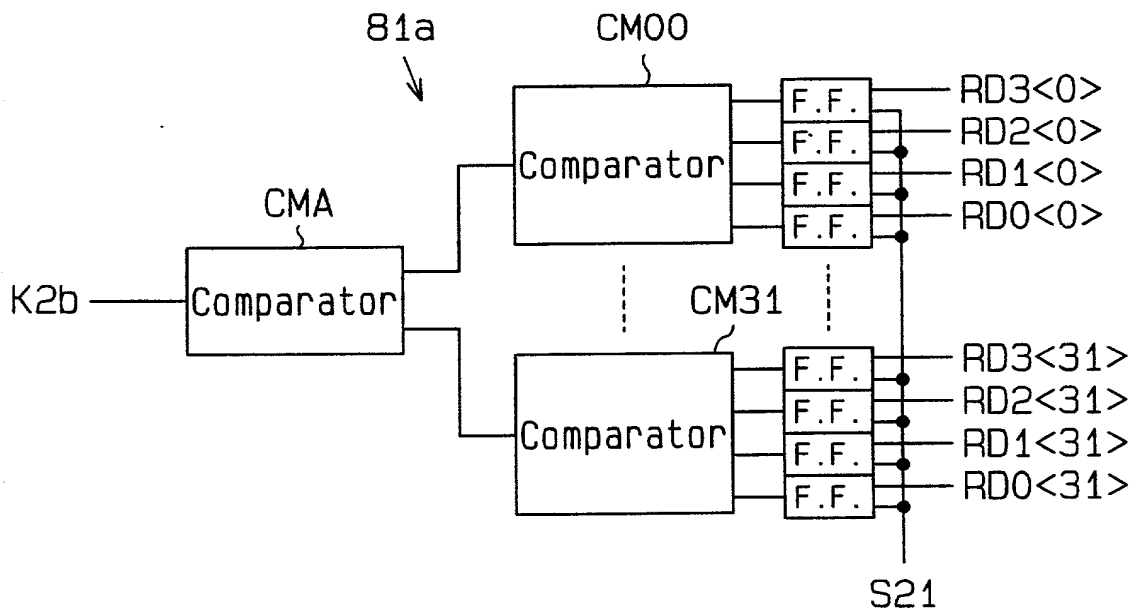


Fig.15

